TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/586,800
Filing Date	July 13, 2006
First Named Inventor	Yongxiang Han
Art Unit	2616
Examiner Name	
Attorney Docket Number	42P21623

Total Number of Pages in This Submission

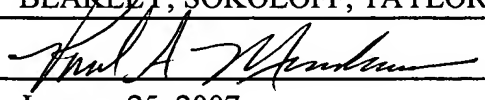
ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [x] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below):*

-Return postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Paul A. Mendonsa, Reg. No. 42,879 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	January 25, 2007

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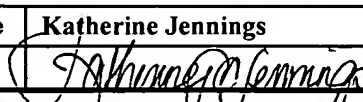
Typed or printed name	Katherine Jennings		
Signature		Date	January 25, 2007

FEE TRANSMITTAL for FY 2006

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)

Complete if Known	
Application Number	10/586,800
Filing Date	July 13, 2006
First Named Inventor	Yongxiang Han
Examiner Name	
Art Unit	2616
Attorney Docket No.	42P21623

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☒ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.
☐ Credit any overpayments

FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($)

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Paul A. Mendonsa	Registration No. (Attorney/Agent)	42,879	Telephone	(503) 439-8778
Signature				Date	01/25/07

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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OF THE PEOPLE'S REPUBLIC OF CHINA

证 明

CERTIFICATE

本证明之附件是向中国专利局作为受理局提交的下列国际申请副本

HIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY OF THE BELOW IDENTIFIED INTERNATIONAL APPLICATION THAT WAS FILED WITH THE CHINESE PATENT OFFICE AS RECEIVING OFFICE

际 申 请 号: PCT/CN2005/001594

RNATIONAL APPLICATION NUMBER

际 申 请 日: 28. SEP 2005 (28. 09. 2005)

NATILNAL FILING DATE

明 名 称: UPDATING ENTRIES CACHED BY A NETWORK PROCESSOR

OF INVENTION

CERTIFIED COPY OF
PRIORITY DOCUMENT

BEST AVAILABLE COPY

中华人民共和国国家知识产权局局长

COMMISSIONER OF THE STATE INTELLECTUAL PROPERTY OFFECE OF THE PEOPLE'S REPUBLIC OF CHINA

二零零七年一月五日

PCT

REQUEST

HOME COPY

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No. PCT/CN 2005 / 0 0 1 5 9 4

International Filing Date 28 · SEP 2005 (2 8 · 0 9 · 2 0 0 5)

Name of receiving Office and "PCT International Application" RO/CN 中华人民共和国国家知识产权局 PCT International Application

Applicant's or agent's file reference *(if desired) (12 characters maximum)* FPEL05150044

Box No. I TITLE OF INVENTION

UPDATING ENTRIES CACHED BY A NETWORK PROCESSOR

Box No. II APPLICANT ☐ This person is also inventor

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

INTEL CORPORATION
2200 Mission College Blvd.
Santa Clara, California 95052
United States of America

Telephone No.

Facsimile No.

Teleprinter No.

Applicant's registration No. with the Office

State *(that is, country)* of nationality: US

State *(that is, country)* of residence: US

This person is applicant for the purposes of: ☐ all designated States ☒ all designated States except the United States of America ☐ the United States of America only ☐ the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

HAN, Yongxiang
6th Floor, North Office Tower, #06-01
Beijing Kerry Centre 1, Guanghua Road
Chaoyang District, Beijing 100020
P. R. of China

This person is:
☐ applicant only
☒ applicant and inventor
☐ inventor only *(If this check-box is marked, do not fill in below.)*

Applicant's registration No. with the Office

State *(that is, country)* of nationality: US

State *(that is, country)* of residence: US

This person is applicant for the purposes of: ☐ all designated States ☐ all designated States except the United States of America ☒ the United States of America only ☐ the States indicated in the Supplemental Box

☒ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as: ☒ agent ☐ common representative

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)*

China Patent Agent (H.K.) Ltd.
22/F, Great Eagle Centre
23 Harbour Road, Wanchai
Hong Kong Special Administrative Region
The People's Republic of China

Telephone No. (852)28284688

Facsimile No. (852)28271018

Teleprinter No.

Agent's registration No. with the Office

☐ **Address for correspondence:** Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Continuation of Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

If none of the following sub-boxes is used, this sheet should not be included in the request.

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

ZHANG, Yu
6th Floor, North Office Tower, #06-01
Beijing Kerry Centre 1, Guanghua Road
Chaoyang District, Beijing 100020
P. R. of China

This person is:
- ☐ applicant only
- ☒ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

Applicant's registration No. with the Office:

State *(that is, country)* of nationality: CN

State *(that is, country)* of residence: CN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☒ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

YU, Zhihong
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Chaoyang District, Beijing 100020
P. R. of China

This person is:
- ☐ applicant only
- ☒ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

Applicant's registration No. with the Office:

State *(that is, country)* of nationality: CN

State *(that is, country)* of residence: CN

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☒ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- ☐ applicant only
- ☐ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

Applicant's registration No. with the Office:

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☐ the United States of America only
- ☐ the States indicated in the Supplemental Box

Name and address: *(Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)*

This person is:
- ☐ applicant only
- ☐ applicant and inventor
- ☐ inventor only *(If this check-box is marked, do not fill in below.)*

Applicant's registration No. with the Office:

State *(that is, country)* of nationality:

State *(that is, country)* of residence:

This person is applicant for the purposes of:
- ☐ all designated States
- ☐ all designated States except the United States of America
- ☐ the United States of America only
- ☐ the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on another continuation sheet.

Box No. V DESIGNATIONS

The filing of this request **constitutes under Rule 4.9(a), the designation** of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.

However,

☐ DE Germany **is not designated** for any kind of national protection

☐ KR Republic of Korea **is not designated** for any kind of national protection

☐ RU Russian Federation **is not designated** for any kind of national protection

(The check-boxes above may be used to exclude (irrevocably) the designations concerned in order to avoid the ceasing of the effect, under the national law, of an earlier national application from which priority is claimed. See the Notes to Box No. V as to the consequences of such national law provisions in these and certain other States.)

Box No. VI PRIORITY CLAIM

The priority of the following earlier application(s) is hereby claimed:

Filing date of earlier application *(day/month/year)*	Number of earlier application	Where earlier application is:		
		national application: country or Member of WTO	regional application:* regional Office	international application: receiving Office
item (1)				
item (2)				
item (3)				

☐ Further priority claims are indicated in the Supplemental Box.

The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) *(only if the earlier application was filed with the Office which for the purposes of this international application is the receiving Office)* identified above as:

☐ all items ☐ item (1) ☐ item (2) ☐ item (3) ☐ other, see Supplemental Box

** Where the earlier application is an ARIPO application, indicate at least one country party to the Paris Convention for the Protection of Industrial Property or one Member of the World Trade Organization for which that earlier application was filed (Rule 4.10(b)(ii)):* . . . .

. . . . . .

Box No. VII INTERNATIONAL SEARCHING AUTHORITY

Choice of International Searching Authority (ISA) *(if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used):*

ISA / CN . . . . . .

Request to use results of earlier search; reference to that search *(if an earlier search has been carried out by or requested from the International Searching Authority):*

Date *(day/month/year)* Number Country *(or regional Office)*

Box No. VIII DECLARATIONS

The following **declarations** are contained in Boxes Nos. VIII (i) to (v) *(mark the applicable check-boxes below and indicate in the right column the number of each type of declaration)*:		Number of declarations
☐ Box No. VIII (i)	Declaration as to the identity of the inventor :	
☐ Box No. VIII (ii)	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent :	
☐ Box No. VIII (iii)	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application :	
☐ Box No. VIII (iv)	Declaration of inventorship (only for the purposes of the designation of the United States of America) :	
☐ Box No. VIII (v)	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty :	

Box No. IX CHECK LIST; LANGUAGE OF FILING

This international application **contains:**

(a) **in paper form,** the following number of sheets:

request (including declaration sheets)	:	4
description (excluding sequence listing and/or tables related thereto)	:	12
claims	:	7
abstract	:	1
drawings	:	Δ 5 ~~[4]~~
Sub-total number of sheets	:	Δ 29 ~~[28]~~
sequence listing	:	
tables related thereto	:	
(for both, actual number of sheets if filed in paper form, whether or not also filed in computer readable form; see (c) below)		
Total number of sheets	:	Δ 29 ~~[28]~~

(b) ☐ **only in computer readable form** (Section 801(a)(i))
- (i) ☐ sequence listing
- (ii) ☐ tables related thereto

(c) ☐ **also in computer readable form** (Section 801(a)(ii))
- (i) ☐ sequence listing
- (ii) ☐ tables related thereto

Type and number of carriers (diskette, CD-ROM, CD-R or other) on which are contained the
- ☐ sequence listing: .....
- ☐ tables related thereto: .....

(additional copies to be indicated under items 9(ii) and/or 10(ii), in right column)

This international application is **accompanied by** the following item(s) *(mark the applicable check-boxes below and indicate in right column the number of each item):*

		Number of items
1. ☒	fee calculation sheet	: 1
2. ☒	original separate power of attorney	: 1
3. ☐	original general power of attorney	:
4. ☐	copy of general power of attorney; reference number, if any:	:
5. ☐	statement explaining lack of signature	:
6. ☐	priority document(s) identified in Box No. VI as item(s):	:
7. ☐	translation of international application into *(language)*:	:
8. ☐	separate indications concerning deposited microorganism or other biological material	:
9. ☐	sequence listing in computer readable form *(indicate type and number of carriers)*	
(i) ☐	copy submitted for the purposes of international search under Rule 13*ter* only (and not as part of the international application)	:
(ii) ☐	*(only where check-box (b)(i) or (c)(i) is marked in left column)* additional copies including, where applicable, the copy for the purposes of international search under Rule 13*ter*	:
(iii) ☐	together with relevant statement as to the identity of the copy or copies with the sequence listing mentioned in left column	:
10. ☐	tables in computer readable form related to sequence listing *(indicate type and number of carriers)*	
(i) ☐	copy submitted for the purposes of international search under Section 802(b-*quater*) only (and not as part of the international application)	:
(ii) ☐	*(only where check-box (b)(ii) or (c)(ii) is marked in left column)* additional copies including, where applicable, the copy for the purposes of international search under Section 802(b-*quater*)	:
(iii) ☐	together with relevant statement as to the identity of the copy or copies with the tables mentioned in left column	:
11. ☐	other *(specify)*:	:

Figure of the drawings which should accompany the abstract:

Language of filing of the international application: EN

Box No. X SIGNATURE OF APPLICANT, AGENT OR COMMON REPRESENTATIVE

Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request).

CHINA PATENT AGENT (HONG KONG) LIMITED 中國專利代理(香港)有限公司 專用章

For receiving Office use only

1. Date of actual receipt of the purported international application: 28 SEP 2005 (28.09.2005)		2. Drawings: ☐ received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:		
4. Date of timely receipt of the required corrections under PCT Article 11(2):		☐ not received:
5. International Searching Authority (if two or more are competent): ISA /	6. ☐ Transmittal of search copy delayed until search fee is paid	

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Date of receipt of the record copy by the International Bureau:

This sheet is not part of and does not count as a sheet of the international application.

PCT

FEE CALCULATION SHEET

Annex to the Request

For receiving Office use only

PCT/CN 2005 / 0 0 1 5 9 4
International Application No.

28 · SEP 2005 (28 · 09 · 2005)
Date stamp of the receiving Office

Applicant's or agent's file reference: FPEL05150044

Applicant: INTEL CORPORATION etc.

CALCULATION OF PRESCRIBED FEES

1. TRANSMITTAL FEE	CNY500	T	CNY500
2. SEARCH FEE	CNY1500	S	CNY1500
International search to be carried out by: CN			
(If two or more International Searching Authorities are competent to carry out the international search, indicate the name of the Authority which is chosen to carry out the international search.)			
3. INTERNATIONAL FILING FEE			
Where items (b) and/or (c) of Box No. IX apply, enter **Sub-total number of sheets** Where items (b) and (c) of Box No. IX do not apply, enter **Total number of sheets**: 28			
i1 first 30 sheets	CHF1400	i1	CHF1400
i2 ____ (number of sheets in excess of 30) x ____ (fee per sheet) =		i2	
i3 additional component (only if sequence listing and/or tables related thereto are filed in computer readable form under Section 801(a)(i), or both in that form and on paper, under Section 801(a)(ii)):			
400 x ____ (fee per sheet) =		i3	
Add amounts entered at i1, i2 and i3 and enter total at I	CHF1400	I	CHF1400
(Applicants from certain States are entitled to a reduction of 75% of the international filing fee. Where the applicant is (or all applicants are) so entitled, the total to be entered at I is 25% of the international filing fee.)			
4. FEE FOR PRIORITY DOCUMENT *(if applicable)*		P	
5. TOTAL FEES PAYABLE Add amounts entered at T, S, I and P, and enter total in the TOTAL box	CNY2000CHF1400 TOTAL		CNY2000 CHF1400

MODE OF PAYMENT

- [X] authorization to charge deposit account (see below)
- [ ] postal money order
- [ ] cash
- [ ] coupons
- [ ] cheque
- [ ] bank draft
- [ ] revenue stamps
- [ ] other *(specify)*:

AUTHORIZATION TO CHARGE (OR CREDIT) DEPOSIT ACCOUNT

(This mode of payment may not be available at all receiving Offices)

- [X] Authorization to charge the total fees indicated above.
- [X] *(This check-box may be marked only if the conditions for deposit accounts of the receiving Office so permit)* Authorization to charge any deficiency or credit any overpayment in the total fees indicated above.
- [X] Authorization to charge the fee for priority document.

Receiving Office: CN

Deposit Account No.:

Date: 09/29/2005

Name:

Signature:

CHINA PATENT AGENT (HONG KONG) LIMITED 中國專利代理(香港)有限公司 專用章

See Notes to the fee calculation sheet

PCT/CN 2005 / 0 0 1 5 9 4

UPDATING ENTRIES CACHED BY A NETWORK PROCESSOR

BACKGROUND

[0001] A network communication system transmits information in packets from a transmitter to a receiver through one or more routers which route the packets between nodes within a network or between networks. The router may comprise one or more network processors to process and forward the packets to different destinations, and one or more external memories to store entries used by the network processors, such as node configuration data, packet queue and flow configuration data, etc.

[0002] The network processor may comprise a control plane to setup, configure and update the entries in the external memories, and a data plane having a plurality of microengines to process and forward the packets by utilizing the entries. Each of the microengines may have a local memory to store entries of the external memories that are frequently used. Once the control plane updates entries in the external memory, it may send a signal to the microengine(s) of the data plane that may cache or store the updated entries in its local memory. In response to the signal, the microengine(s) may flush all entries stored in the local memory to make them consistent with entries stored in the external memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The invention described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to

other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0004] Fig. 1 shows an embodiment of a network device.

[0005] Fig. 2 shows an embodiment of a network processor of the network device of Fig. 1.

[0006] Fig. 3 shows an embodiment of a method implemented by a control plane of the network processor depicted in FIG. 2.

[0007] Fig. 4 shows an embodiment of another method implemented by a microengine of the network processor depicted in FIG. 2.

[0008] Fig. 5 shows a data flow diagram of an embodiment for updating entries cached by the network processor depicted in FIG. 2.

DETAILED DESCRIPTION

[0009] The following description describes techniques for updating entries cached in a network processor. In the following description, numerous specific details such as logic implementations, pseudo-code, means to specify operands, resource partitioning/sharing/duplication implementations, types and interrelationships of system components, and logic partitioning/integration choices are set forth in order to provide a more thorough understanding of the current invention. However, the invention may be practiced without such specific details. In other instances, control structures, gate level circuits and full software instruction sequences have not been shown in detail in order not to obscure the invention. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate functionality without undue experimentation.

[0010] References in the specification to "one embodiment", "an embodiment", "an example embodiment", etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0011] Embodiments of the invention may be implemented in hardware, firmware, software, or any combination thereof. Embodiments of the invention may also be implemented as instructions stored on a machine-readable medium, that may be read and executed by one or more processors. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.) and others.

[0012] An embodiment of a network device 8 to route packets of a network communication system is shown in Fig. 1. The network device 8 may comprise a network interface 10, a framer 11, one or more network processors 12/13, a switch fabric 14, and one or more external memories 15/16. Examples for the network device 8 may comprise an ATM switch (Asynchronous Transfer Mode),

an IP router (Internet Protocol), a SDH DXC (Synchronous Digital Hierarchy Data-cross Connection), and the like.

[0013] The framer 11 may perform operations on frames. In an embodiment, the framer 11 may receive a line datagram from a network interface 10 of the network communication system, delimitate frames and extract payload, such as Ethernet packet from the frames. In another embodiment, the framer 11 may receive packets from network processor 13, encapsulate the packets into frames and map the frames onto the network interface 10. The framer 11 may further perform operations such as error detection and/or correction. Examples for the framer 11 may comprise a POS (packet over Synchronous Optic Network) framer, a High-Level Data Link (HDLC) framer or the like.

[0014] The network processors 12 and 13 may perform operations on packets. In an embodiment, the network processor 12 may process and forward the packets from the framer 11 to an appropriate port of another network device through the switch fabric 14. For example, the network processor 12 may assemble IPv4 (Internet Protocol version 4) packets into CSIX (Common Switch Interface Specification) packets, modify packet headers and payloads, determine appropriate ports and forward the CSIX packets to the appropriate ports of the another network device. The network processor 13 may process and forward packets from the switch fabric 14 to appropriate ports 20 of the network interface 10 through the framer 11. For example, the network processor 13 may reassemble CSIX packets into IPv4 packets, modify packet headers and payloads, determine appropriate ports 20 and forward the IPv4 datagrams to the appropriate ports 20. Examples for the network processors 12 and 13 may comprise Intel® IXP 2XXX (e.g., IXP2400, IXP2800) network processors.

[0015] The switch fabric 14 may receive and send packets from/to a network processor connected therewith. Examples for the switch fabric 14 may comprise a switch fabric conforming to CSIX or other fabric technologies such as HyperTransport, Infiniband, PCI-X, Packet-Over-Synchronous Optical Network, RapidIO, and Utopia.

[0016] The external memories 15 and 16 may store entries 155/165 used by the network processors 12 and 13 to process and forward the packets. The entries may comprise node configuration data, queue configuration data, flow configuration data, network routing data, etc. The external memories 15 and 16 may further buffer the packets. In one embodiment, the external memory 15/16 may comprise SDRAM (Synchronous Dynamic Random Access memory) to store packets and QDR SRAM (Quad Data Rate Static Random Access Memory) to store entries.

[0017] Other embodiments may implement other modifications and variations on the structure of the network device as depicted in Fig. 1. For instance, the network processors 12 and 13 may perform framing duties instead of the framer 11 and the switch fabric may be omitted in a single-box scenario. For another instance, the network processors 12 and 13 may be integrated as one.

[0018] An embodiment of the network processor 12 (or network processor 13) is shown in Fig. 2. As shown, the network processor 12 may comprise a control plane 211, a data plane 212 and a scratch pad 213 that are communicable with each other through a bus connection.

[0019] The control plane 211 may be implemented as an integrated circuit (IC) with one or more processing cores 214_1 ... 214_M such Intel® XScale® processing cores or StrongARM® processing cores to execute instructions to perform various

tasks. In an embodiment, the processing cores 214_1 ... 214_M of the control plane 211 may execute instructions to setup, configure and update entries 155/165 stored in the external memories 15/16. For instance, the processing cores 214_1 ... 214_M may update the external memories 15/16 which contain entries such as, for example, configuration data for nodes, configuration data for each packet queue, configuration data for each packet flow, etc. In another embodiment, the processing cores 214_1 ... 214_M may further handle packets containing protocol message and routing information that may need relatively complex computations. For instance, the processing cores 214_1 ... 214_M may process routing protocol packets containing routing information such as, for example, RIP (Routing Information Protocol) packets, OSPF (Open Shortest Path First) packets, and the like.

[0020] The data plane 212 may comprise a plurality of microengines 215_1 ... 215_N in Fig. 2 that may be communicable with each other. Each of the microengines may comprise a plurality of threads 216_1 ... 216_K to process and forward packets and one or more local memories 218_1 ... 218_N to store instruction code 220 and entries 224. The local memory 218_1 ... 218_N may comprise a control store, a memory, general purpose registers, transfer registers, and/or other storage mechanisms. In an embodiment, the local memories 218_1 ... 218_N may comprise instruction code 220 executable by the threads 216_1 ... 216_K and one or more entries 224 consistent with the entries 155/165 of the external memories 15/16. The threads 216_1 ... 216_K may access the local memories 218_1 ... 218_N to fetch some useful information for packet forwarding. Entries 155/165 may be cached from the external memory 15/16 to the local memories 218_1 ... 218_N of the microengines 215_1 ... 215_N based upon some criteria, for example, whether the

entries 155/165 are frequently used by one or more microengines 215_1 ... 215_N of the data plane 212. Further, the entries 155/165 cached by one microengine 215_1 ... 215_N may be different from the entries 155/165 cached by another microengine 215_1 ... 215_N.

[0021] The scratch pad 213 is accessible by both the processing cores 214_1 ... 214_M of the control plane 211 and the microengines 215_1 ... 215_N of the data plane 212. The scratch pad 213 may comprise a buffer 226_1 ... 226_N to store data for each microengines 215_1 ... 215_N. The buffers 226_1 ... 226_N may be implemented using various structures such as, for example, ring buffers, link lists, stacks, etc. In other embodiments, the scratch pad 215 may be regarded as a flat memory.

[0022] In an embodiment, processing cores 214_1 ... 214_M of the control plane 211 may update one or more entries 155/165 in the external memories 15/16 by adding, deleting or changing one or more entries 155/165, and may write information related to the updated entries 155/165 to each buffer 226_1 ... 226_N of the scratch pad 213 associated with a microengine 215_1 ... 251_N that stores the updated entries 155/165 in its local memory 218_1 ... 218_N. Then, the microengines 215_1 ... 215_N may extract information from its buffer 226_1 ... 226_N, read the updated entries 155/165 from the external memories 15/16 and update the corresponding entries 224 in the local memories 218_1 ... 218_N. The information written in the buffers 226_1 ... 226_N may comprise entry identifiers (e.g. addresses, entry numbers, entry pointers) that uniquely identify entries 155/165 of the external memories 15/16.

[0023] Other embodiments may implement other modifications and variations on the structure of the network processor as depicted in Fig. 2. For example, the

network processor 12 may further comprise a hash engine, a peripheral component interconnect (PCI) bus interface for communicating, etc.

[0024] Fig. 3 shows a process implemented by one or more processing cores 214_1 ... 214_M of the control plane 211 to update an external entry 155/165 stored in an external memory 15/16. As shown, in block 301, the control plane 211 may update an entry 155 in the external memory 15. Then, in block 302, the control plane 211 may search for microengine(s) 215_1 ... 215_N of the data plane 212 affected by the updated entry 155. In one embodiment, the control plane 211 determines a microengine 215_1 ... 215_N is affected by the updated entry 155 by determining that the microengine 215_1 ... 215_N has the updated entry 155 cached in its corresponding local memory 218_1 ... 218_N.

[0025] The control plane 211 may implement block 302 in various ways. In an embodiment, the control plane 211 may determine the affected microengines 215_1 ... 215_N by referring to a table of the external memory 15/16 or scratch pad 213 that lists the microengines 215_1 ... 215_N having cached a particular external entry 155. For example, the control plane 211 may supply a CAM (content addressable memory) of the external memory 15 with an identifier (e.g. an address, index, hash value, etc.) for the updated entry 155 to obtain a list of microengines 215_1 ... 215_N that have the entry 155 cached. In particular, the CAM may return a data word having at least N bits wherein each bit indicates whether a corresponding microengine 215_1 ... 215_N has the updated entry 155 cached. However, it should be appreciated that the control plane 211 may utilize other techniques and structures to maintain a corresponds between entries 155/165 and the microengines 215_1 ... 215_N that have stored local copies of the entries 155/165.

[0026] In block 303, the control plane 211 may write information associated with the external entry 155 updated in block 301 to buffers 226_1 ... 226_N of microengines 215_1 ... 215_N affected by the updated entry 155. The information may comprise identifiers that identify external entry 155/165 that have been updated by the control plane 211.

[0027] For instance, if an entry 155 of external table 151 is updated in block 301, the control plane 211 may search for the microengines 215_1 ... 215_N. that store the entry 155 in their local memories 218_1 ... 218_N (block 302). Then, the control plane 211 in block 303 may write an identifier (e.g. address, entry number, entry pointer, and/or other data) for the updated entry 155 to the buffers 226_1 ... 226_N of the affected microengines 215_1 ... 215_N identified in block 302. For example, if the control plane 211 determines in block 302 that microengines 215_1 and 215_N have cached the updated entry 155, then the control plane 211 in block 303 may write an identifier for the entry 155 to the corresponding buffers 226_1 and 226_N to inform the microengines 215_1 and 215_N that the identified entry 155 has been updated.

[0028] In another embodiment, if all entries or more than a threshold level of entries of the external memory 15 are updated in block 301, the control plane 211 may forgo block 302 and write a wildcard identifier to the buffers 226_1 ... 226_N indicating all cached entries 155 of the external memory 15 are invalid or outdated.

[0029] Fig. 4 shows an embodiment of a method to update one ore more entries 224 of local memories 218_1 ... 218_N of the data plane microengines 215_1 ... 215_N. In block 402, one thread 216_1 ... 216_K of each microengine 215_1 ... 215_N of the data plane 212 may be designated or otherwise configured to perform the task of updating cached entries 224 of the microengine 215_1 ... 215_N. In one

embodiment, the control plane 211 may designate a thread 216_1 ... 216_K of each microengine 215_1 ... 215_N that is to update the cached entries 224 of the microengine 215_1 ... 215_N. Other embodiments may utilize other techniques to designate the thread to update the cached entries 224. For example, the microengine 215_1 ... 215_N may designate the thread, the thread may be predetermined by the instruction code 220, and/or the thread designation may be hardwired into the microengine 215_1 ... 215_N. In block 404, a thread 216_1 ... 216_K of a microengine 215_1 ... 215_N may be selected to continue executing its assigned tasks. To this end, the microengine 215_1 ... 215_N and/or the control plane 211 may awaken and/or otherwise activate the selected thread using various thread scheduling algorithms such as, for example, round robin, priority, weighted priority, and/or other scheduling algorithms.

[0030] In block 406, the selected thread 216_1 ... 216_K may determine whether the selected thread 216_1 ... 216_K is designated to update the local memory 218_1 ... 218_N of its microengine 215_1 ... 215_N. If selected thread 216_1 ... 216_K determines in block 406 that another thread 216_1 ... 216_K is designated for updates, then the selected thread 216_1 ... 216_K in block 408 may continue to process packets in a normal fashion. If, however, the selected thread 216_1 ... 216_K is designated to update its local memory 218_1 ... 218_N, then the thread 216_1 ... 216_K in block 410 may determine whether the buffer 226_1 ... 226_K for its microengine 215_1 ... 215_N indicates that entries 226 are invalid or outdated.

[0031] The selected thread 216_1 ... 216_K may implement block 410 in various ways. For an embodiment wherein the buffers 226_1 ... 226_N are scratch rings, the selected thread 216_1 ... 216_K may execute a predetermined instruction (e.g. 'br_!inp_state[...]') of the instruction code 220 and may determine whether a

returned value of the predetermined instruction is true ('1') or false ('0'). The selected thread 216_1 ... 216_K may determine no updates are pending if the returned value is false, and likewise may determine one or more entries 226 of its local memory 218_1 ... 218_N are to be updated if the returned value is true.

[0032] If the selected thread 216_1 ... 216_K determines to update entries 224 of its local memory 218_1 ... 218_N, the thread 216_1 ... 216_K in block 412 may extract identifiers for the updated entries 155/165 from the buffer 226_1 ... 226_N associated with the microengine 215_1 ... 215_N of the thread 216_1 ... 216_K. The information may comprise an entry identifier that uniquely identifies the updated entries 155/165 of the external memories 15/16. Such an identifier may comprise an external memory number, an external memory pointer, an entry number, an entry pointer, and/or other identifying information from which an entry 155/165 may be discerned. However, if the selected thread 216_1 ... 216_K determines to update no entries 224 of its local memory 218_1 ... 218_N, the selected thread 216_1 ... 216_K may continue to block 408 to perform normal packet processing.

[0033] In block 414, the selected thread 216_1 ... 216_K may read entries 155/165 from the external memory 15/16 that have been identified by information in its corresponding buffer 226_1 ... 226_N as being updated. Further, the selected thread 216_1 ... 216_K may update corresponding cached entries 224 based upon the entries read from the external memory 15/16 (block 416).

[0034] Other embodiments may implement other modifications and variations to the process as depicted in Fig. 4. For example, a microengine 215_1 ... 215_N may not assign a single thread 216_1 ... 216_K to perform the task of updating local memory 218_1 ... 218_N. Instead, each thread 216_1 ... 216_K of the microengine 215_1

... 215_N may determine whether to update entries 224 cached in its local memory 218_1 ... 218_N before continuing with normal packet processing.

[0035] A data flow diagram illustrating an embodiment of updating entries 224 of local memories 218_1 ... 218_N of the network processor 12 is shown in Fig. 5. As shown, the control plane 211 may update one or more external entries 155 in an external memory 15 (arrow 501). Then, the control plane 211 may write information associated with the updated external entries 155 to the buffers 226_1 ... 226_N assigned to the affected microengines 215_1 ... 215_N (arrow 502). In response to a thread 216_1 ... 216_K determining, based upon information stored in its buffers 218_1 ... 218_N, that one or more cached entries 224 of its microengine 215_1 ... 215_N have been updated, the thread 216_1 ...216_K may read the updated external entries 155 from the external memory 15 (arrow 504) and update the corresponding local memory 218_1 ... 218_N with the read entries 155 (arrow 505).

[0036] While certain features of the invention have been described with reference to example embodiments, the description is not intended to be construed in a limiting sense. Various modifications of the example embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

What is claimed is:

1. A method of a network processor comprising a plurality of microengines that process network packets, the method comprising

updating an entry in a memory external to the network processor;

identifying a microengine of the plurality of microengines that has stored the entry in a local memory for the microengine; and

writing information to a buffer for the identified microengine that indicates the entry has been updated.

2. The method of claim 1 further comprising updating the entry in the local memory for the microengine in response to determining, based upon the information written to the buffer, that the entry has been updated.

3. The method of claim 1 further comprising

reading the entry from the memory external to the network processor in response to determining, based upon the information written to the buffer, that the entry has been updated; and

updating the local memory for the microengine based upon the entry read from the memory external to the network processor.

4. The method of claim 1 further comprising

updating the entry in the local memory for the microengine in response to determining, based upon the information written to the buffer, that the entry has been updated; and

processing a network packet based upon the entry updated in the local memory for the microengine.

5. The method of claim 1 further comprising designating at least one thread of each microengine of the plurality of microengines to update entries of a corresponding local memory for each microengine based upon information stored in a corresponding buffer for each microengine.

6. The method of claim 1 further comprising activating a thread of the microengine to process information stored in the buffer and to update the local memory of the microengine based upon the information stored in the buffer.

7. The method of claim 1 further comprising determining that all entries in the local memory for the microengine are invalid based upon the information stored in the buffer for the microengine.

8. The method of claim 1 further comprising determining that all entries in the local memory for the microengine are outdated based upon the information stored in the buffer for the microengine.

9. A network processor to process network packets based upon entries stored in an external memory, comprising:

a plurality of microengines to process network packets, each microengine having a corresponding local memory to cache entries stored in the external memory and a corresponding buffer to identify entries in the local memory updated in the external memory, and

a control plane to update an entry in the external memory, to identify each microengine of the plurality of microengines having the entry stored in the corresponding local memory, and to store an identifier for the entry in the corresponding buffer for each identified microengine to indicate that the entry has been updated in the external memory.

10. The network processor of claim 9 wherein the control plane comprises at least one processing core to update the entry, to identify each microengine, and to store the identifier in the corresponding buffer for each identified microengine.

11. The network processor of claim 9 wherein each microengine

reads the entry from the external memory in response to determining, based upon the identifier written to the corresponding buffer, that the entry has been updated, and

updates the corresponding local memory based upon the entry read from the external memory.

12. The network processor of claim 9 wherein each microengine

updates the entry in the corresponding local memory in response to determining, based upon the identifier written to the corresponding buffer, that the entry has been updated, and

processes a network packet based upon the entry updated in the corresponding local memory.

13. The network processor of claim 9 wherein each microengine comprises a plurality of threads to process network packets and at least one thread to update entries of the corresponding local memory upon identifiers for entries stored in the corresponding buffer.

14. A network device, comprising:

a plurality of ports to transfer network packets;

a memory to store entries used to process network packets;

a network processor to process network packets based upon the entries stored in the memory external to the network processor, wherein the network processor comprises

a plurality of microengines to process network packets, each microengine having a corresponding local memory to cache entries stored in the external memory and a corresponding buffer to identify entries in the local memory updated in the external memory, and

at least one processing core to control the plurality of microengines, to update entries in the memory external to the network processor, to identify each microengine of the plurality of microengines having updated entries of the memory stored in corresponding local memory, and to store information in the corresponding buffer for each identified microengine to indicate updated entries of the memory.

15. The network device of claim 14 wherein each microengine

reads updated entries from the memory based upon the information in the corresponding buffer, and

updates the corresponding local memory based upon the updated entries read from the memory.

16. The network device of claim 14 wherein each microengine

updates entries in the corresponding local memory based upon information in their corresponding buffer, and

processes network packets based upon the entries updated in the corresponding local memory.

17. The network device of claim 14 wherein each microengine comprises a plurality of threads to process network packets, wherein at least one thread of the plurality of threads updates entries of the corresponding local memory based upon information in the corresponding buffer.

18. The network device of claim 14 wherein

each microengine comprises a plurality of threads to process network packets, and

the at least one processing core designates at least one thread of each microengine to update entries of the corresponding local memory of the microengine based upon information in the corresponding buffer of the microengine.

19. A machine readable medium comprising a plurality of instructions that in response to being executed result in a network device

updating an entry in a memory external to a network processor of the network device;

identifying each microengine of the network processor that has cached the entry in a local memory of the network processor;

storing information to a corresponding buffer for each identified microengine, the information indicating the entry has been updated in the memory external to the network processor; and

updating the entry cached in the local memory based upon the information in the corresponding buffer for each identified microengine.

20. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device

reading the entry from the memory external to the network processor in response to determining, based upon the information written to the buffer, that the entry has been updated; and

updating the entry cached in the local memory based upon the entry read from the memory external to the network processor.

21. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device processing a network packet based upon the updated entry cached in the local memory.

22. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device designating at least one thread of each microengine of the plurality of microengines to update entries of the local memory based upon information stored in the corresponding buffer for each microengine.

ABSTRACT

Machine-readable media, methods, and apparatus are described to update entries cached in a network processor. In some embodiments, microengines of a network processor cache entries in corresponding local memories and update cached entries based upon information stored in corresponding buffers for the microengines. A control plane of the network processor identifies each microengine having updated entry stored in corresponding local memory, and store information in the corresponding buffer for each identified microengine to indicate that the entry has been updated in the external memory.

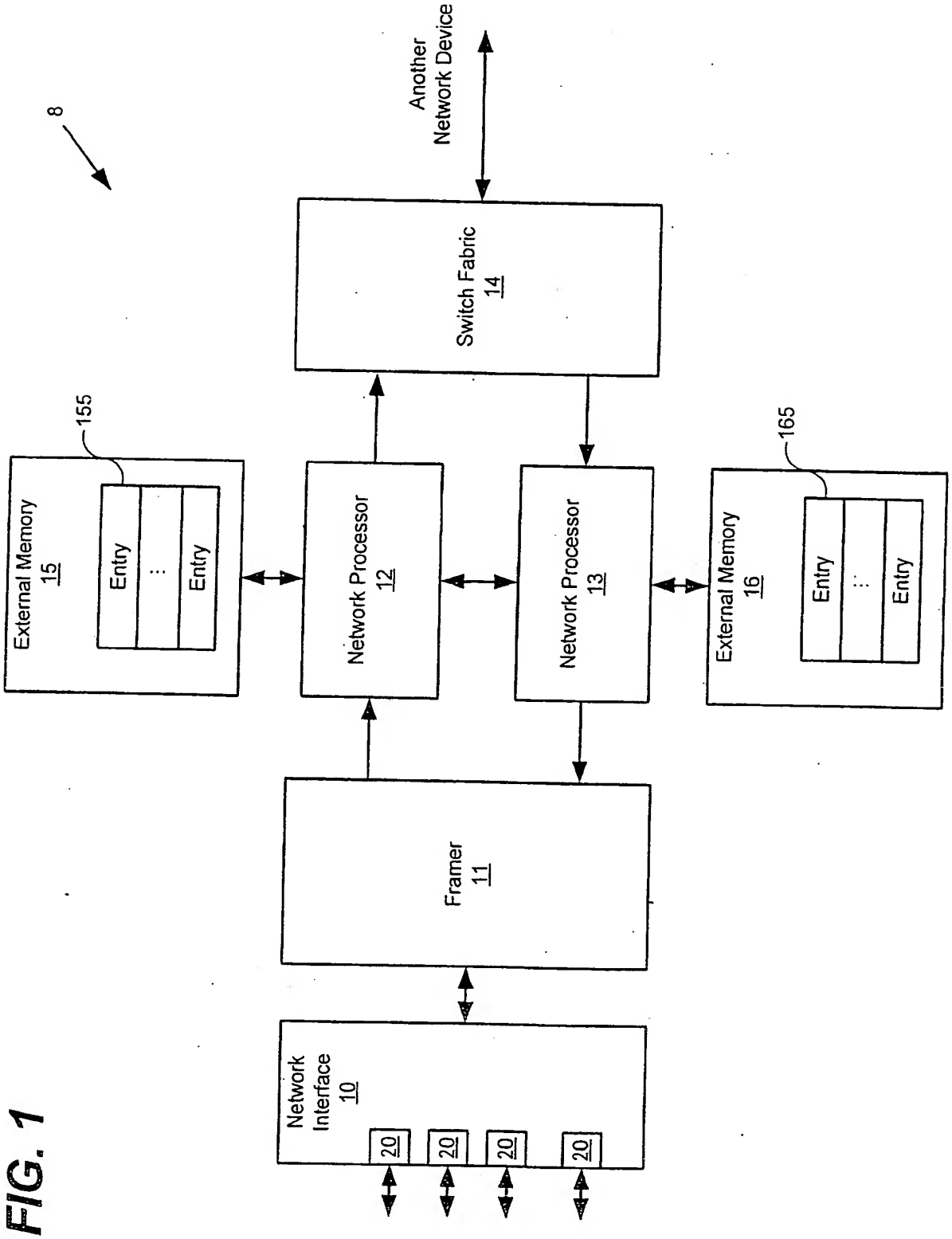

8
Another Network Device
Switch Fabric 14
155
External Memory 15
Entry
Entry
Network Processor 12
Network Processor 13
165
External Memory 16
Entry
Entry
Framer 11
Network Interface 10
20
20
20
20

FIG. 1

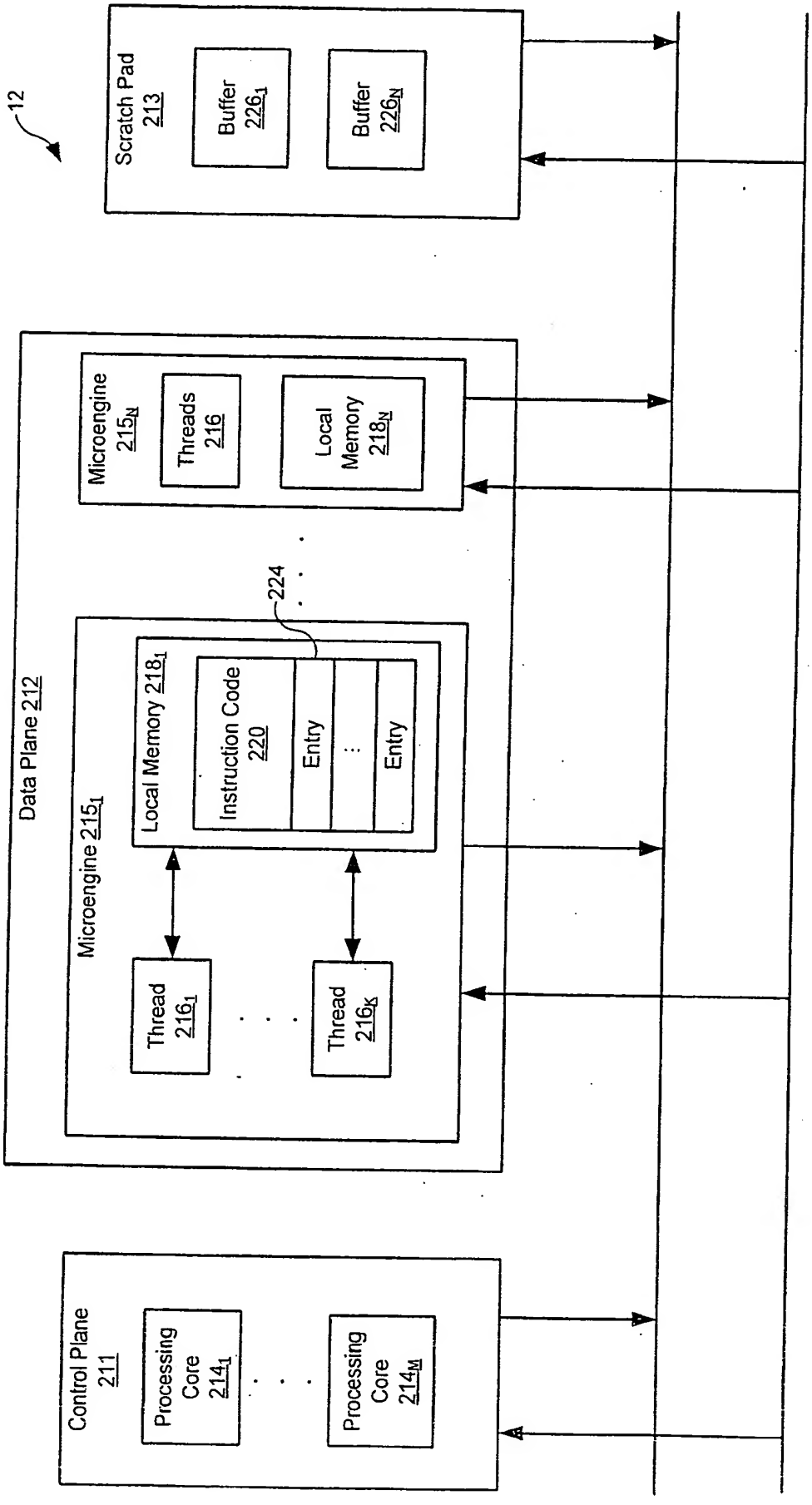

12
Scratch Pad 213
Buffer 226$_1$
Buffer 226$_N$
Data Plane 212
Microengine 215$_N$
Threads 216
Local Memory 218$_N$
224
Microengine 215$_1$
Local Memory 218$_1$
Instruction Code 220
Entry
Entry
Thread 216$_1$
Thread 216$_K$
Control Plane 211
Processing Core 214$_1$
Processing Core 214$_M$

FIG. 2

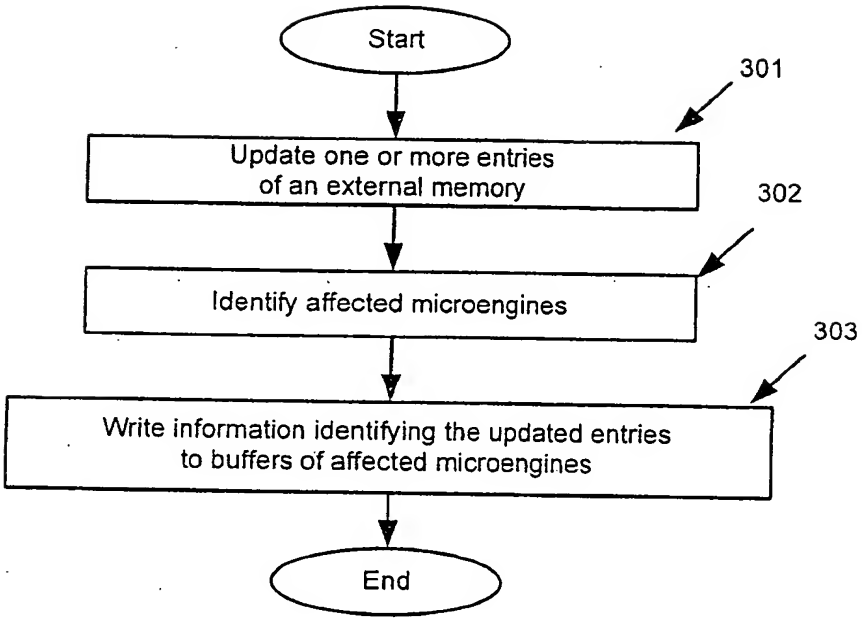

Start
301
Update one or more entries of an external memory
302
Identify affected microengines
303
Write information identifying the updated entries to buffers of affected microengines
End

FIG. 3

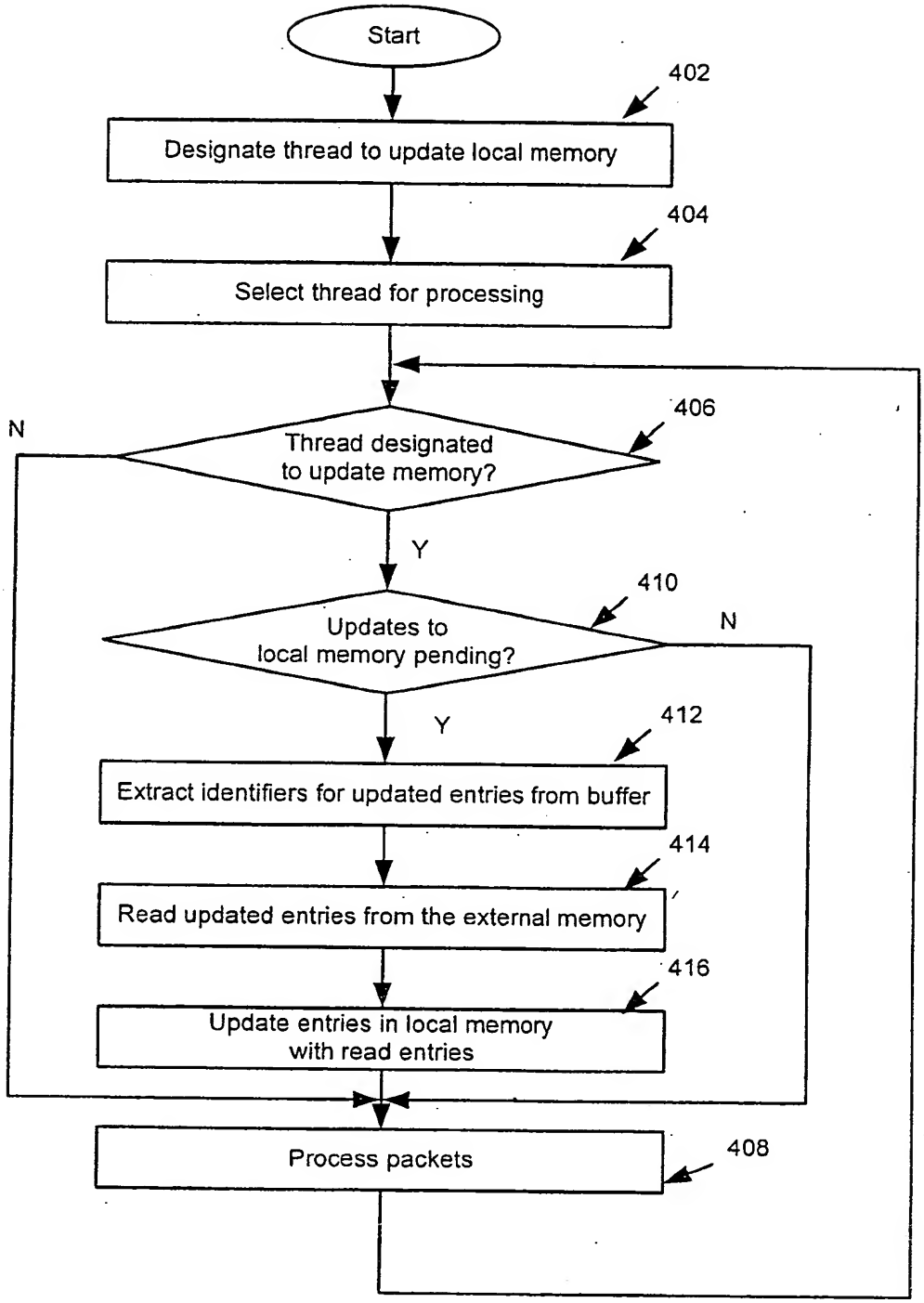
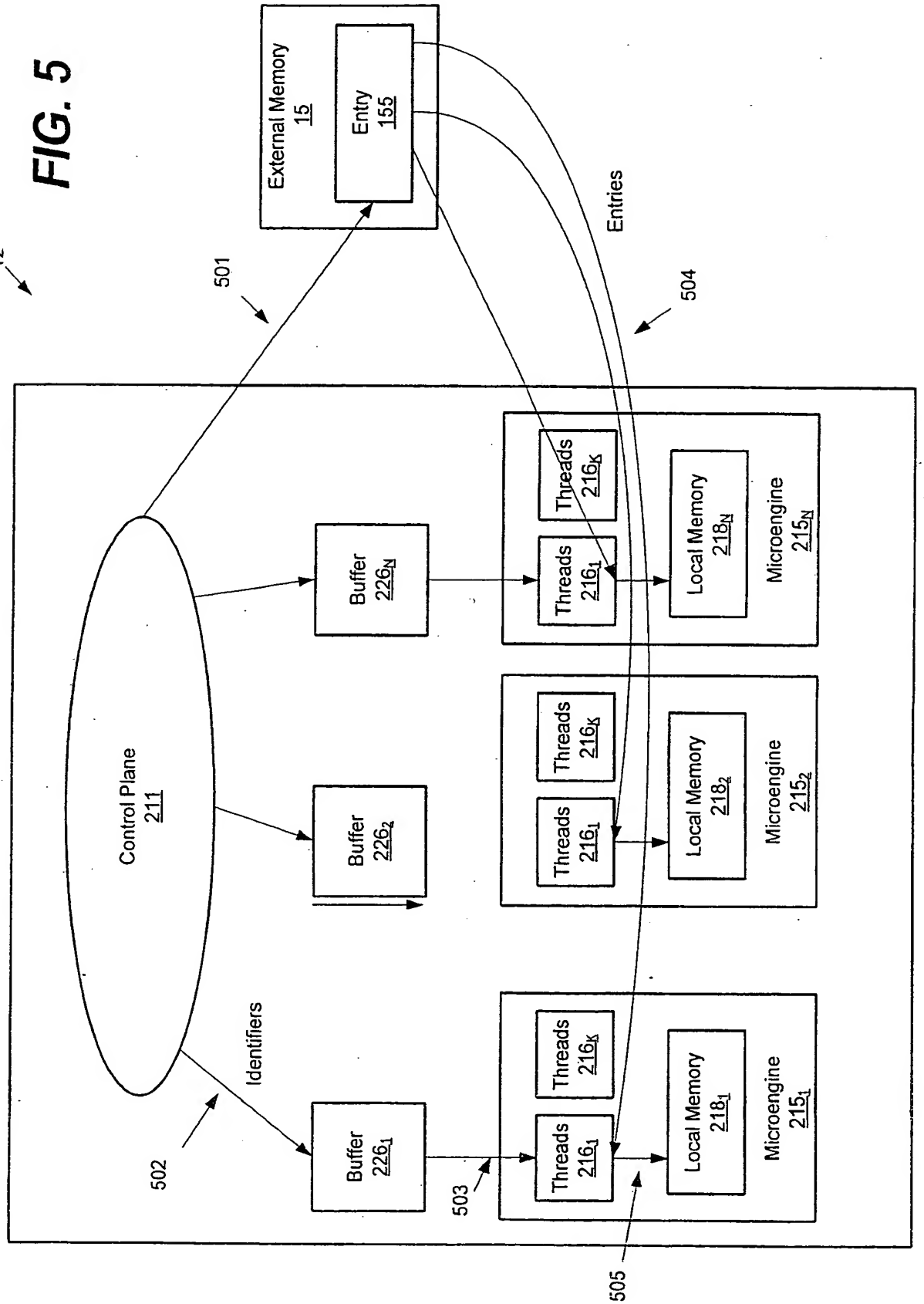

Start
402
Designate thread to update local memory
404
Select thread for processing
406
Thread designated to update memory?
N
Y
410
Updates to local memory pending?
N
Y
412
Extract identifiers for updated entries from buffer
414
Read updated entries from the external memory
416
Update entries in local memory with read entries
Process packets
408

FIG. 4

FIG. 5


12
External Memory 15
Entry 155
501
Entries
504
Control Plane 211
Buffer 226N
Buffer 226₂
Buffer 226₁
Identifiers
502
503
505
Threads 216K
Threads 216₁
Local Memory 218N
Microengine 215N
Local Memory 218₂
Microengine 215₂
Local Memory 218₁
Microengine 215₁